

Substitute for form 1449A/PTO				Complete if Known	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (use as many sheets as necessary)				Application Number	<del>Not Yet Assigned</del> 10695927
				Filing Date	October 30, 2003
				First Named Inventor	Yukihisa KINUGASA
				Art Unit	<del>Not Yet Assigned</del> 2816
				Examiner Name	<del>Not Yet Assigned</del> Wells
Sheet	1	of	1	Attorney Docket Number	031794-5

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	U.S. Patent Documents	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
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FOREIGN PATENT DOCUMENTS						
Examiner Initials <sup>*</sup>	Cite No. <sup>1</sup>	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code <sup>3</sup>	Number <sup>4</sup> Kind Code <sup>5</sup> (if known)			
Can		JP	11-88071 A	03/30/1999	T. Harada et al	W/Abstract
Can		JP	2001-44770 A	02/16/2001	K. Komatsu et al	W/Abstract

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials <sup>*</sup>	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
Can		"Neuron-MOS Current Mirror Circuit and Its Application to Multi-Valued Logic" Jing SHEN et al. IEICE TRANS. INF. & SYST., VOL. E82-D, No. 5 May 1999 (pp 940-948)	

Examiner Signature	WELLS	Date Considered	6/10/04
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